REMARKS

The Applicant sincerely appreciates the Examiner's thorough examination of the present application as evidenced by the final Office Action of December 11, 2006 ("the Office Action"). In particular, the Applicant appreciates the withdrawal of all prior rejections. In response to the new rejections presented in the Office Action, the Applicant will show in the following remarks that all claims are patentable over the cited art. Accordingly, the Applicant respectfully submits that all claims are in condition for allowance, and a Notice of Allowance is respectfully requested in due course.

The Subject Matter Of Claims 8 And 59 Is Believed To Be Patentable

The Applicant believes that the subject matter of dependent Claim 8 and independent Claim 59 is allowable because no rejections have been applied to these claims. The Applicants have not rewritten Claim 8 in independent form because the Applicant will show in the following remarks that independent Claim 1 (from which Claim 8 depends) is patentable.

Independent Claims 1, 9, 15, 19, 21, 22, 27, 29, 42, 52, and 75 Are Patentable Over The Combination Of Jones, Bertin, And Perino

Claims 1, 9, 15, 19, 21, 22, 27, 29, 42, 52, and 75 have been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over U.S. Patent No. 6,731,009 to Jones et al. (Jones) in view of U.S. Patent No. 5,977,640 to Bertin et al. (Bertin) and U.S. Patent No. 6,621,155 to Perino et al. (Perino). The Applicant respectfully submits, however, that these claims are patentable for at least the reasons discussed below. Claim 1, for example, recites an electronic device comprising:

> a first integrated circuit substrate;
> a second integrated circuit substrate on the first integrated circuit substrate;
> a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;
> a first electrical and mechanical connection between the first and third integrated circuit substrates wherein the first electrical and mechanical connection bypasses the second integrated circuit substrate;
> a second electrical and mechanical connection between the second and third integrated circuit substrates; and

> a third electrical and mechanical connection between the first and second integrated circuit substrates.

The Office Action concedes that:

> Fig. 3C of Jones shows most aspect of the instant invention except a first electrical and mechanical connection between the first and third integrated circuit substrates wherein the first electrical bypasses the second integrated circuit substrate; a second electrical connection between the second and third integrated circuit electronic substrates; and a third electrical between the first and second integrated circuit substrates. (Underline added.)

Office Action, page 3. In support of the rejection, the Office Action states that:

> Fig. 16 of Bertin shows that an electrical connection (bumps) between the first and the third IC's 40, 40A bypassing the second IC and the second IC 30, 30A electrically connected to the first and third. It would have been obvious ... to modify Jones with Bertin by an electrical connection between the first and third bypassing the second and the second IC electrically connected to the first and the third for compact package. (Underline added.)

Office Action, page 3.

The Office Action thus appears to take the position that it would be obvious to somehow modify the multi-chip assembly 318 from Figure 3C of Jones using the using the chips 40 and 40A from Figure 16 of Bertin so that an electrical interconnection is provided between the first die 308-0 and the third die 308-2 from Figure 3C of Jones bypassing the second die 308-1 from Figure 3C of Jones. The Applicant respectfully disagrees. As shown in Figure 3C of Jones, active sides of each of the die 308-0, 308-1, and 308-2 face the substrate 302 (*i.e.*, the die 308-0, 308-1, and 308-2 face the same direction) to facilitate electrical connection between each of the dies 308-0, 308-1, and 308-2 and the substrate 302. In contrast, Figure 16 of Bertin shows that chips 40 and 40A face each other.

Accordingly, it would not be obvious to insert the interconnection substrate 88A and/or the coupling substrate 88B from Figure 16 of Bertin to provide electrical connection between the first and third die 308-0 and 308-2 from Figure 3C of Jones because:

(1) the first and third die 308-0 and 308-2 from Figure 3C of Jones are separated by the second die 308-1 preventing the interconnection suggested by the Office Action; and
(2) the interconnection substrate 88A and the coupling substrate 88B of Figure 16 of Bertin that connect chips 40 and 40A that face each other would not work to connect the die

> 308-0 and 308-2 of Figure 3C of Jones that both face (and are electrically connected to) the substrate 302.

Accordingly, there is no suggestion or motivation in the prior art to combine elements of Jones and Bertin as suggested in the Office Action as is required by Section 2143 of the Manual Of Patent Examining Procedure (MPEP). Moreover, even if elements of Jones and Bertin are combined as suggested by the Office Action, there is no reasonable expectation of success as further required by Section 2143 of the MPEP. Accordingly, the Office Action fails to meet the requirements for a *prima facie* case of obviousness as set forth in MPEP Sec. 2143.

Regarding Perino, the Office Action states that:

> The combination of Jones/Bertin fails to show a mechanical connection between the IC's. Fig. 3D of Perino shows a mechanical connection (495's; interposer) between the three IC's and all the IC's have the same size. It would have been obvious ... to modify Jones/Bertin with Perino by a mechanical connection and the same size of the IC' to secure the package and the same size of the IC's
>
> Note that the combination of Jones/Bertin/Perino shows all the aspect regarding the first, second and third IC's and Fig. 3D of Perino shows a connection between the multiple layers of IC's. In addition, Fig. 3D of Perino shows an electrical connection between the IC's and the top IC's and the first bottom IC are connected to the signal via the circuit board. Therefore, the combination of Jones/Bertin/Perino shows a direct electrical coupling between the IC's.

Office Action, page 3.

As discussed above, it would not be obvious to combine Jones and Bertin as suggested by the Office Action. Accepting for the sake of argument, however, that Jones and Bertin are combined as suggested by the Office Action, it would not be obvious to combine Perino with Jones and Bertin to provide the still missing teachings as suggested by the Office Action. In particular, Figure 3D of Perino shows a structure with conductors 440a-440h between IC die using wire bonding or flexible circuit tape. *See*, Perino, col. 6, lines 5-19. In contrast, substrate connections 310 and 312 in Figure 3C of Jones include conductive bumps to form a flip-chip type arrangement (*see*, Jones, col. 6, lines 3-5), and connections between chips 30, 30A, 40, and 40A in Figure 16 of Bertin are provided using interconnection substrate 88A, coupling substrate 88B, and solder balls. Accordingly, it would not be obvious to selectively combine elements of wirebonded and soldered structures to somehow teach or suggest the electronic device of Claim 1.

The Applicant thus submits that the combination of Jones, Bertin, and Perino fails to teach or suggest the recitations of Claim 1 and that Claim 1 is thus patentable. The Applicant further submits that independent Claims 9, 15, 19, 21, 22, 27, 29, 42, 52, 59, and 75 are patentable for reasons similar to those discussed above with respect to Claim 1. In addition, dependent Claims 2-4, 6-8, 10-14, 16-18, 23-26, 28, 30-31, 33-40, 43-51, 55-58, 60, 62-74, and 76-79 are patentable at least as per the patentability of the independent claims from which they depend.

Claims 7, 9, 15, and 19 Are Separately Patentable Over The Combination Of Jones, Bertin, And Perino

Claims 7, 9, 15, and 19 have been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over U.S. Patent No. 6,731,009 to Jones et al. (Jones) in view of U.S. Patent No. 5,977,640 to Bertin et al. (Bertin) and U.S. Patent No. 6,621,155 to Perino et al. (Perino). These claims, however, are patentable for at least the reasons discussed above with respect to Claim 1. The Applicant further submits that these claims are separately patentable for at least the additional reasons discussed below. Claim 9, for example, recites an electronic device comprising:

> a first integrated circuit substrate;
> a second integrated circuit substrate on the first integrated circuit substrate;
> a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;
> a first conductive bump between the first and third integrated circuit substrates wherein the first conductive bump is spaced apart from and extends past an edge of the second integrated circuit substrate wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates; and
> a second conductive bump between the second and third integrated circuit substrates wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates;
> wherein each of the first, second, and third integrated circuit substrates includes a device side having electronic circuits thereon and a backside, wherein the device sides of the first, second, and third integrated circuit substrates face a first direction, and the backsides of the first, second, and third integrated circuit substrates face a second direction.

As set forth in the Manual Of Patent Examining Procedure, to establish a *prima facie* case of obviousness, the prior art references when combined must teach or suggest all the claim limitations. *See*, MPEP, Sec. 2143. The Applicants respectfully submit that none of Jones, Bertin, and/or Perino, taken alone or in combination, teaches or suggests the first conductive bump of Claim 9. More particularly, the cited references (taken alone or in combination) fail to teach or suggest a conductive bump between first and third integrated circuit substrates wherein the first conductive bump is spaced apart from and extends past an edge of a second integrated circuit substrate (between the first and third integrated circuit substrates) and wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates. In Figure 3C of Jones, none of the substrate connections 310, 312, and/or 322 provides electrical and mechanical interconnection between die 308-0, 308-1, and/or 308-2. In Figure 16 of Bertin, none of the circular connections extends past an edge of either of the chips 30 and/or 30A. Moreover, it would not be obvious to somehow selectively combine elements of Figure 3C of Jones (with die 308-0, 308-1, and/or 308-2 facing and coupled to a substrate 302) and elements of Figure 16 of Bertin (with chips 40 and 40A facing and coupled to each other) as discussed above with respect to Claim 1. Moreover, Figure 3D of Perino fails to provide any missing teachings relating to the first conductive bump of Claim 9 because conductors 440a-440j are formed using wire bonding or flexible circuit tape. *See*, Perino, col. 6, lines 15-16.

For at least the reasons discussed above, the Applicant respectfully submits that Claim 9 is separately patentable over the combination of Jones, Bertin, and Perino. The Applicant further submits that Claims 7, 15, and 19 are patentable for reasons similar to those discussed above with respect to Claim 9. In addition, dependent Claims 8, 10-14, 16-18, and 64-71 are patentable at least as per the patentability of Claims 7, 9, 15, and 19 from which they depend.

Claims 15, 31, 36, 45, 67, and 76 Are Separately Patentable
Over The Combination Of Jones, Bertin, And Perino

Claims 15, 31, 36, 45, 67, and 76 have been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over U.S. Patent No. 6,731,009 to Jones et al. (Jones) in view of U.S. Patent No. 5,977,640 to Bertin et al. (Bertin) and U.S. Patent No. 6,621,155 to Perino et al. (Perino).

These claims, however, are patentable for at least the reasons discussed above with respect to Claim 1. The Applicant further submits that these claims are separately patentable for at least the additional reasons discussed below. Claim 15, for example, recites an electronic device comprising:

> a first integrated circuit substrate;
> a second integrated circuit substrate on the first integrated circuit substrate;
> a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates;
> a first conductive bump between the first and third integrated circuit substrates wherein the first conductive bump is spaced apart from and extends past an edge of the second integrated circuit substrate wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates; ...
> a printed circuit board, wherein the first, second, and third integrated circuit substrates have device sides facing the printed circuit board and backsides facing away from the printed circuit board; .... (Underline added.)

As set forth in the Manual Of Patent Examining Procedure, to establish a *prima facie* case of obviousness, the prior art references when combined must teach or suggest all the claim limitations. *See*, MPEP, Sec. 2143. The Applicants respectfully submit that none of Jones, Bertin, and/or Perino, taken alone or in combination, teaches or suggests a conductive bump providing electrical and mechanical connection between two integrated circuit substrates facing a same direction. Neither of Jones or Perino teaches or suggests a conductive bump between two integrated circuit substrates, much less a conductive bump between two integrated circuit substrates facing a same direction. To the extent that Figure 16 of Bertin shows a conductive bump providing electrical and mechanical connection between two integrated circuit substrates, Bertin shows such an electrical and mechanical connection between two integrated circuit substrates that are facing each other (and not facing a same direction).

For at least the reasons discussed above, the Applicant respectfully submits that Claim 15 is separately patentable over the combination of Jones, Bertin, and Perino. In addition, the Applicant submits that Claims 31, 36, 45, 67, and 76 are separately patentable for reasons similar to those discussed above with respect to Claim 15. In addition, dependent Claims 16-18, 33, 37-39, 46-49, and 77-79 are patentable at least as per the patentability of Claims 15, 31, 36, 45, 67, and 76 from which they depend.

Claim 28 Is Separately Patentable
Over The Combination Of Jones, Bertin, And Perino

Claim 28 has been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over U.S. Patent No. 6,731,009 to Jones et al. (Jones) in view of U.S. Patent No. 5,977,640 to Bertin et al. (Bertin) and U.S. Patent No. 6,621,155 to Perino et al. (Perino). This claim, however, is patentable for at least the reasons discussed above with respect to Claim 1. The Applicant further submits that this claim is separately patentable for at least the additional reasons discussed below. Claim 28 depends from Claim 27, and thus includes all recitations of Claim 27. In addition, Claim 28 (including all recitations of Claim 27 from which it depends) recites an electronic device comprising:

> a printed circuit board;
> a first integrated circuit substrate on the printed circuit board;
> a second integrated circuit substrate on the first integrated circuit substrate wherein the first integrated circuit substrate is between the printed circuit board and the second integrated circuit substrate;
> a third integrated circuit substrate on the second integrated circuit substrate wherein the second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the second integrated circuit substrate is offset relative to the first and third integrated circuit substrates so that the first and third integrated circuit substrates extend beyond an end of the second integrated circuit substrate;
> a first conductive bump between the first and third integrated circuit substrates, wherein the first conductive bump provides electrical and mechanical connection between the first and third integrated circuit substrates; and
> a second conductive bump between the second and third integrated circuit substrates, wherein the second conductive bump provides electrical and mechanical connection between the second and third integrated circuit substrates;
> wherein the first, second, and third integrated circuit substrates have a same size…
> … wherein the first conductive bump has a greater volume than the second conductive bump. (Recitations of Claim 28 underlined.)

As set forth in the Manual Of Patent Examining Procedure, to establish a *prima facie* case of obviousness, the prior art references when combined must teach or suggest all the claim limitations. *See*, MPEP, Sec. 2143. The Applicants respectfully submit that none of Jones, Bertin, and/or Perino, taken alone or in combination, teaches or suggests conductive bumps between integrated circuit substrates having different volumes. Figure 3C of Jones fails to teach

or suggest conductive bumps between integrated circuit substrates, much less conductive bumps of different volumes between integrated circuit substrates. To the extent that Figure 16 of Bertin shows conductive bumps between integrated circuits, any such conductive bumps of Bertin would appear to have a same volume. As discussed above, Figure 3D of Perino shows conductors 440a-j formed using wire bonding of flexible circuit tape. *See*, Perino, col. 6, lines 15-16.

For at least the reasons discussed above, the Applicant respectfully submits that Claim 28 is separately patentable over the combination of Jones, Bertin, and Perino. In addition, the Applicant submits that Claim 8 is separately patentable for reasons similar to those discussed above with respect to Claim 28.

Claims 42 And 52 Are Separately Patentable
Over The Combination Of Jones, Bertin, And Perino

Claims 42 and 52 have been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over U.S. Patent No. 6,731,009 to Jones et al. (Jones) in view of U.S. Patent No. 5,977,640 to Bertin et al. (Bertin) and U.S. Patent No. 6,621,155 to Perino et al. (Perino). These claims, however, are patentable for at least the reasons discussed above with respect to Claim 1. The Applicant further submits that these claims are separately patentable for at least the additional reasons discussed below. Claim 42, for example, recites an electronic device comprising:

> a first integrated circuit substrate having opposing first and second surfaces;
> a second integrated circuit substrate on the first integrated circuit substrate, the second integrated circuit substrate having opposing first and second surfaces;
> a third integrated circuit substrate on the second integrated circuit substrate, the third integrated circuit substrate having opposing first and second surfaces, wherein the second integrated circuit substrate is between the first and third integrated circuit substrates, wherein the first surface of the second integrated circuit substrate faces the second surface of the first integrated circuit substrate, and wherein the second surface of the second integrated circuit substrate faces the first surface of the third integrated circuit substrate; and
> a signal path extending along a first conductive trace on the first surface of the second integrated circuit substrate, to the second surface of the first integrated circuit substrate, along a second conductive trace on the second surface of the first integrated circuit substrate, to the first surface of the third integrated circuit substrate, along a third conductive trace on the first surface of the third integrated circuit substrate, and to the second surface of the second integrated circuit substrate. (Underline added.)

As set forth in the Manual Of Patent Examining Procedure, to establish a *prima facie* case of obviousness, the prior art references when combined must teach or suggest all the claim limitations. *See*, MPEP, Sec. 2143. The Applicants respectfully submit that none of Jones, Bertin, and/or Perino, taken alone or in combination, teaches or suggests a signal path including conductive traces on opposing first and second surfaces of a same integrated circuit substrate. Regarding Figure 3C of Jones, nothing in Jones teaches or suggests conductive traces on opposite sides of any of the die 308-0, 308-1, and/or 308-2. Regarding Figure 16 of Bertin, nothing in Bertin teaches or suggests conductive traces on opposite sides of any of the chips 03, 30A, 40, and/or 40A. Regarding Figure 3D of Perino, nothing in Perino teaches or suggests conductive traces on opposite sides of any of the IC die 410a-h and/or 495a-h.

For at least the reasons discussed above, the Applicant respectfully submits that Claim 42 is separately patentable over the combination of Jones, Bertin, and Perino. In addition, the Applicant submits that Claims 52, and 59 are separately patentable for reasons similar to those discussed above with respect to Claim 42. In addition, dependent Claims 43-51, 55-58, 60, 63, and 74 are patentable at least as per the patentability of Claims 42, 52, and 59 from which they depend.

CONCLUSION

Accordingly, the Applicant submits that all pending claims in the present application are in condition for allowance, and a Notice of Allowance is respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone should any additional issues need to be addressed.

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